

# SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

SREE SAINATH NAGAR, TIRUPATI – 517 102

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

SVEC/CSE/2011-12

Date: 30-06-2011

## TIME TABLE ACADEMIC YEAR 2011-2012 II B.Tech - Semester - I - Section B

Room No. 134

w.e.f. 04-07-2011

HOUR / DAY	11:00 11:50	11:50 12:40	12:40 1:30		2:15 3:05	3:05 3:55	3:55 4:45
MON	BEE	DMS	EDC	B R E A K	PS	DLD	DS
TUE	PS	EDC	DLD		DS LAB (A&B LABS)		
WED	DS	BEE	EDC		DLD	DMS	PS
THU	DLD	PS	EDC		BEE	DS	DMS
FRI	DMS	DS	PS		BEE	EDC	DLD
SAT	ADE LAB				DS	DMS	BEE

P & S	PROBABILITY AND STATISTICS	Mr. K.A. AJMATH
EDC	ELECTRONIC DEVICES AND CIRCUITS	Ms. A. SRIVIDYA
BEE	BASIC ELECTRICAL ENGINEERING	Mr. B.SUBBA REDDY
DLD	DIGITAL LOGIC DESIGN	Mr.P.VENKATESWARLU REDDY
DMS	DISCRETE MATHEMATICAL STRUCTURES	Ms. P. RAJANI
DS	DATA STRUCTURES	Mr. B. NARENDRA KUMAR RAO

ADE LAB	ANALOG AND DIGITAL ELECTRONICS LAB
DS LAB	DATA STRUCTURES LAB

ASV	IS	PVR
BNKR	KMVP	MAK
LVR		

HOD, CSE

PRINCIPAL