



# SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

Sree Sainath Nagar, Tirupati – 517 102

## Department of Electronics and Communication Engineering

### Course Structure for M. Tech. (VLSI)

#### M. Tech. – I Semester

Subject Code	Name of the Subject	L+T	P	Internal Marks	External Marks	Total Marks	C
10MT15701	Analog IC Design	4	-	40	60	100	4
10MT15702	Digital Design Modeling and Synthesis with HDLs	4	-	40	60	100	4
10MT15703	Digital IC Design	4	-	40	60	100	4
10MT15704	Hardware Software Co-Design	4	-	40	60	100	4
10MT15705	VLSI Technology	4	-	40	60	100	4
<b>Elective-I</b>							
10MT15706	ASIC Design	4	-	40	60	100	4
10MT15707	Embedded Systems						
10MT15708	System Modeling and Simulation						
10MT15709	Digital IC Design Lab.	-	4	25	50	75	2
<b>Total</b>		<b>24</b>	<b>4</b>	<b>265</b>	<b>410</b>	<b>675</b>	<b>26</b>

#### M. Tech. – II Semester

Subject Code	Name of the Subject	L+T	P	Internal Marks	External Marks	Total Marks	C
10MT25701	Algorithms for VLSI Physical Design Automation	4	-	40	60	100	4
10MT25702	CPLD & FPGA Architectures and Applications	4	-	40	60	100	4
10MT25703	Digital System Testing and Testability	4	-	40	60	100	4
10MT25704	Low Power VLSI Design	4	-	40	60	100	4
10MT25705	Scripting Language for VLSI Design Automation	4	-	40	60	100	4
<b>Elective-II</b>							
10MT25706	Cryptography and Network Security	4	-	40	60	100	4
10MT25707	Nano Electronics						
10MT25708	Real Time Operating Systems						
10MT25709	Industrial Visit/ Mini-Project/ Seminar	-	-	50	-	50	2
10MT25710	Mixed Signal Lab.	-	4	25	50	75	2
<b>Total</b>		<b>24</b>	<b>4</b>	<b>315</b>	<b>410</b>	<b>725</b>	<b>28</b>

#### M. Tech. – III Semester

Subject Code	Name of the Subject	L+T	P	Internal Marks	External Marks	Total Marks	C
10MT35701	Project Work – Phase I	-	-	50	-	50	4
<b>Total</b>				<b>50</b>	<b>-</b>	<b>50</b>	<b>4</b>

#### M. Tech. – IV Semester

Subject Code	Name of the Subject	L+T	P	Internal Marks	External Marks	Total Marks	C
10MT45701	Project Work – Phase II	-	-	50	100	150	12
<b>Total</b>				<b>50</b>	<b>100</b>	<b>150</b>	<b>12</b>

**Total Marks : 1600**

**Total Credits: 70**

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**M. Tech. (VLSI)  
I SEMESTER**

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## **(10MT15701) ANALOG IC DESIGN**

### **UNIT I**

MOS transistors-modeling in linear, saturation and cutoff high frequency equivalent circuit.

### **UNIT II & III**

#### **INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR:**

Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

### **UNIT IV**

**OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION:** Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded-Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator . Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

### **UNIT V**

**SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I:** MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

### **UNIT VI**

**SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-II:** Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

### **UNIT VII**

**DATA CONVERTERS:** Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating ,Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

### **UNIT VIII**

**OVER SAMPLING CONVERTERS AND FILTERS:** Over Sampling With and Without Noise Shaping. Digital Decimation Filter. High Order Modulators. Band Pass Over Sampling Converter. Practical Considerations. Continuous Time Filters.

**TEXT BOOKS:**

1. D.A.John & Ken Martin, "Analog Integrated Circuit Design", John Wiley, 1997.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata-Mc GrawHill, 2002.

**REFERENCES:**

1. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.
2. Gregolian & Temes, "Analog MOS Integrated Circuits", John Wiley, 1986.

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## **(10MT15702) DIGITAL DESIGN MODELLING AND SYNTHESIS WITH HDLS**

### **UNIT I**

**HARDWARE MODELING WITH THE VERILOG HDL:** Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

### **UNIT II**

**LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL:** User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

### **UNIT III**

**BEHAVIORAL DESCRIPTIONS IN VERILOG HDL:** Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

### **UNIT IV**

**SYNTHESIS OF COMBINATIONAL LOGIC:** HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares, Synthesis of Sequential Logic Synthesis of Sequential Udfs, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

## **UNIT V**

**SYNTHESIS OF LANGUAGE CONSTRUCTS:** Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis of Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

## **UNIT VI**

**SWITCH-LEVEL MODELS IN VERILOG:** MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

## **UNIT VII**

**INTRODUCTION TO VHDL:** An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

## **UNIT VIII**

**BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL:** Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

### **TEXT BOOKS:**

1. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.Nawabi, "VHDL Analysis and Modeling of Digital Systems", McGraw Hill, 2<sup>nd</sup> edition 1998.

### **REFERENCES:**

1. M.G.Arnold, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. Perry, "VHDL", McGraw Hill, 3<sup>rd</sup> edition.

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## **(10MT15703) DIGITAL IC DESIGN**

### **UNIT I**

CMOS inverters -static and dynamic characteristics.

### **UNIT II**

Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

### **UNIT III**

Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design.

### **UNIT IV**

Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

### **UNIT V**

Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

### **UNIT VI&VII**

LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load.

### **UNIT VIII**

**SUBSYSTEM DESIGN PROCESS:** General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

### **TEXT BOOKS:**

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, 2<sup>nd</sup> edition, 1999.
2. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 1997.
3. Eugene D Fabricus, "Introduction to VLSI Design", McGraw Hill International Edition, 1990.

### **REFERENCES:**

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000.
2. Neil H E West and Kamran Eshranghian, "Principles of CMOS VLSI Design: A System Perspective", Addison-Wesley 2<sup>nd</sup> Edition, 2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout and simulation", New York: IEEE Press, 1998.
4. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, "Analysis and Design of Digital Integrated Circuits", McGraw-Hill, 3<sup>rd</sup> Edition, 2004.

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## **(10MT15704) HARDWARE SOFTWARE CO- DESIGN**

### **UNIT I**

**CO- DESIGN ISSUES:** Co- Design Models, Architectures, Languages, a Generic Co-design Methodology.

### **UNIT II**

**CO- SYNTHESIS ALGORITHMS:** Hardware software synthesis algorithms: hardware- software partitioning distributed system co-synthesis.

### **UNIT III**

**PROTOTYPING AND EMULATION:** Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

### **UNIT IV**

**TARGET ARCHITECTURES:** Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

### **UNIT V**

**COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES:** Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

### **UNIT VI**

**DESIGN SPECIFICATION AND VERIFICATION:** Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

### **UNIT VII**

**LANGUAGES FOR SYSTEM- LEVEL SPECIFICATION AND DESIGN-I:** System – level specification, design representation for system level synthesis, system level specification languages,

### **UNIT VIII**

**LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II:** Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

### **TEXT BOOKS:**

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", Springer, 2009.
2. "Hardware / software co-design Principles and Practice", kluwer academic publishers, 2002.

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## **(10MT15705) VLSI TECHNOLOGY**

### **UNIT I**

**REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES:** (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

### **UNIT II**

**BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS:** Ids-Vds Relationships, Threshold Voltage  $V_t$ ,  $G_m$ ,  $G_{ds}$  and  $W_o$ , Pass Transistor, MOS, CMOS & Bi- CMOS Inverters,  $Z_{pu}/Z_{pd}$ , MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

### **UNIT III**

**LAYOUT DESIGN AND TOOLS:** Transistor Structures, Wires and Vias, Scalable Design Rules, Layout Design Tools.

### **UNIT IV**

**LOGIC GATES & LAYOUTS:** Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

### **UNIT V**

**COMBINATIONAL LOGIC NETWORKS:** Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

### **UNIT VI**

**SEQUENTIAL SYSTEMS:** Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

### **UNIT VII**

**FLOOR PLANNING & ARCHITECTURE DESIGN:** Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

### **UNIT VIII**

**INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN:** Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

### **TEXT BOOKS:**

1. K. Eshraghian et. al (3 authors), "Essentials of VLSI Circuits and Systems", PHI of India Ltd., 2005.
2. Wayne Wolf, "Modern VLSI Design", Pearson Education, fifth Indian Reprint, 3rd Edition, 2005.

**REFERENCES:**

1. N.H.E Weste, K.Eshraghian, "Principals of CMOS Design", Adison Wesley, 2nd Edition.
2. Fabricius, "Introduction to VLSI Design", MGH International Edition, 1990.
3. Baker, Li Boyce, "CMOS Circuit Design, Layout and Simulation", PHI, 2004.

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## **(10MT15706) ASIC DESIGN (ELECTIVE I)**

### **UNIT I**

**ASIC DESIGN STYLES:** Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

### **UNIT II**

**ASICS – PROGRAMMABLE LOGIC DEVICES:** Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Intoduction, selected families – design outline.

### **UNIT III**

**ASICS –DESIGN ISSUES:** Design methodologies and design tools – design for testability – economies.

### **UNIT IV**

**ACISS CHARACTERISTICS AND PERFORMANCE:** design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

### **UNIT V**

**ASICS-DESIGN TECHNIQUES:** Overview- Design flow and methodology- Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

### **UNIT VI**

**LOGIC SYNTHESIS, SIMULATION AND TESTING:** Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation.

### **UNIT VII**

**ASIC CONSTRUCTION:** Floor planning, placement and routing system partition.

### **UNIT VIII**

**FPGA PARTITIONING:** Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

### **TEXT BOOKS:**

1. L.J.Herbst, "Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.

### **REFERENCES:**

1. M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman Inc 1997.

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## **(10MT15707) EMBEDDED SYSTEMS (ELECTIVE I)**

### **UNIT I**

**AN INTRODUCTION TO EMBEDDED SYSTEMS:** An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System -On-Chip (SOC) and in VLSI Circuit.

### **UNIT II:**

**PROCESSOR AND MEMORY ORGANIZATION:** Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

### **UNIT III**

**DEVICES AND BUSES FOR DEVICE NETWORKS:** I/O Devices, Timer and Counting Devices, Serial Communication Using The "I<sup>2</sup>C", CAN, Profibus Foundation Field Bus. and Advanced I/O Buses Between the Network Multiple Devices, Host Systems or Computer Parallel Communication between the Networked I/O Multiple Devices using the ISA, PCI, PCI-X and Advanced Buses.

### **UNIT IV**

**DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM:** Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

### **UNIT V**

**INSTRUCTION SETS;** Introduction, preliminaries, ARM processor, SHARC processor.

### **UNIT VI**

**PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++ AND JAVA:** Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

### **UNIT VII & VIII**

**HARDWARE–SOFTWARE CO-DESIGN IN AN EMBEDDED SYSTEM:** Embedded System Project Management, Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, use of Target Systems, use of Software Tools for Development of an Embedded System, use of Scopes and Logic Analysis for System, Hardware Tests. Issues in Embedded System Design.

**TEXTBOOKS:**

1. Rajkamal, "Embedded systems: Architecture, Programming and Design", TMH.
2. Wayne wolf, "Computers as a component: principles of embedded computing system design".

**REFERENCES:**

1. Arnold S Burger, "Embedded system design", CMP.
2. David Simon, "An embedded software primer", PEA.
3. Steve Heath; Butterworth Heinenann, "Embedded systems design:Real world design", Newton mass USA 2002.
4. Hayt, "Data communication".

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**M. Tech. (VLSI)  
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## **(10MT15708) SYSTEM MODELLING AND SIMULATION (ELECTIVE I)**

### **UNIT I**

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative approach to Modeling and Simulation.

### **UNIT II**

**SIMULATION SOFTWARE:** Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

### **UNIT III**

**BUILDING SIMULATION MODELS:** Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

### **UNIT IV**

**MODELING TIME DRIVEN SYSTEMS:** Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

### **UNIT V**

**EXOGENOUS SIGNALS AND EVENTS:** Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

### **UNIT VI**

**MARKOV PROCESS:** Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poisson Process, Continuous-Time Markov Processes.

### **UNIT VII**

**EVENT DRIVEN MODELS:** Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

### **UNIT VIII**

**SYSTEM OPTIMIZATION:** System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

### **TEXT BOOKS:**

1. Frank L. Severance, "System Modeling & Simulation, an Introduction", John Wiley & Sons, 2001.
2. Averill M. Law, W. David Kelton, "Simulation Modeling and Analysis", TMH, 3<sup>rd</sup> Edition, 2003.

### **REFERENCES:**

1. Geoffery Gordon, "Systems Simulation", PHI, 1978.

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**M. Tech. (VLSI)  
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### **(10MT15709) DIGITAL IC DESIGN LABORATORY**

- Digital Circuits Description using Verilog and VHDL.
- Verification of the Functionality of Designed circuits using function Simulator.
- Timing Simulation for critical path time calculation.
- Synthesis of Digital circuits.
- Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
- Implementation of Designed Digital Circuits using FPGA and CPLD devices.

**NOTE:** Required Software Tools:

- Mentor Graphic tools / Cadence tools/ Synopsis tools. (220 nm Technology and Above)
- Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)**

**M. Tech. (VLSI)  
II SEMESTER**

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## **(10MT25701) ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION**

### **UNIT I**

**PRELIMINARIES:** Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

### **UNIT II**

**GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION:** Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

### **UNIT III**

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

### **UNIT IV**

**MODELLING AND SIMULATION:** Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

### **UNIT V**

**LOGIC SYNTHESIS AND VERIFICATION:** Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

### **UNIT VI**

**HIGH-LEVEL SYNTHESIS:** Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

### **UNIT VII**

**PHYSICAL DESIGN AUTOMATION OF FPGA'S:** FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

### **UNIT VIII**

**PHYSICAL DESIGN AUTOMATION OF MCM'S:** MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

### **TEXTBOOKS:**

1. S.H.Gerez, "Algorithms for VLSI Design Automation", WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", Springer International Edition, 3rd edition, 2005.

**REFERENCES:**

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design Systems on silicon", Pearson Education Asia, 2nd Edition, 1998.

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**M. Tech. (VLSI)  
II SEMESTER**

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## **(10MT25702) CPLD AND FPGA ARCHITECTURE AND APPLICATIONS**

### **UNIT I**

**PROGRAMMABLE LOGIC:** ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

### **UNIT II**

**FPGA:** Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

### **UNIT III**

**CASE STUDIES:** Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

### **UNIT IV**

**FINITE STATE MACHINES (FSM):** Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

### **UNIT V**

**REALIZATION OF STATE MACHINE:** Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

### **UNIT VI & VII**

**FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN:** Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

### **UNIT VIII**

**DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS:** Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

**TEXT BOOKS/ REFERENCES:**

1. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
3. J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Publication, 1992.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)**

**M. Tech. (VLSI)  
II SEMESTER**

**L T P C  
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## **(10MT25703) DIGITAL SYSTEM TESTING AND TESTABILITY**

### **UNIT I**

#### **INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT)**

**FUNDAMENTALS:** Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

### **UNIT II**

**FAULT MODELING:** Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

### **UNIT III**

**TESTING FOR SINGLE STUCK FAULTS (SSF):** Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

### **UNIT IV&V**

**DESIGN FOR TESTABILITY:** Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

### **UNIT VI**

**BUILT-IN SELF-TEST (BIST):** BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

### **UNIT VII**

**MEMORY BIST (MBIST):** Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

### **UNIT VIII**

**BRIEF IDEAS ON EMBEDDED CORE TESTING:** Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

### **TEXT BOOKS:**

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.

**REFERENCES:**

1. Alfred Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall.
2. Robert J. Feugate, Jr., Steven M. Mentyn, "Introduction to VLSI Testing", Prentice Hall, Englewood Cliffs, 1998.

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## **(10MT25704) LOW POWER VLSI DESIGN**

### **UNIT I**

**LOW POWER DESIGN, AN OVER VIEW:** Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

### **UNIT II**

**MOS/BiCMOS PROCESSES:** Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

### **UNIT III**

**LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES:** Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

### **UNIT IV**

**DEVICE BEHAVIOR AND MODELING:** Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

### **UNIT V**

**CMOS AND Bi-CMOS LOGIC GATES:** Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

### **UNIT VI**

**LOW- VOLTAGE LOW POWER LOGIC CIRCUITS:** Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

### **UNIT VII**

**LOW POWER LATCHES AND FLIP FLOPS:** Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

### **UNIT VIII**

**SPECIAL TECHNIQUES:** Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

### **TEXT BOOKS:**

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

### **REFERENCES:**

1. Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", PHI, 3<sup>rd</sup> edition.
2. J.Rabaey, "Digital Integrated circuits", PH, 1996.
3. Sung-mo Kang and Yusuf Leblebici, "CMOS Digital ICs", TMH, 3<sup>rd</sup> edition 2003.
4. IEEE Trans Electron Devices, IEEE J. Solid State Circuits, and other National and International Conferences and Symposia.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)**

**M. Tech. (VLSI)  
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## **(10MT25705) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION**

### **UNIT I**

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

### **UNIT II&III**

PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

### **UNIT IV&V**

Inter process Communication Threads, Compilation & Line Interfacing.

### **UNIT VI&VII**

Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.

### **UNIT VIII**

Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

### **TEXT BOOKS:**

1. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly Publications, 3<sup>rd</sup> edition, 2000.
2. Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, 3<sup>rd</sup> edition, 2000.
3. Tom Christiansen, Nathan Torkington, "PERL Cookbook", Oreilly Publications, 3<sup>rd</sup> edition, 2000.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)**

**M. Tech. (VLSI)  
II SEMESTER**

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## **(10MT25706) CRYPTOGRAPHY AND NETWORK SECURITY (ELECTIVE II)**

### **UNIT I**

**SYMMETRIC CIPHERS:** Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

### **UNIT II**

**PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS:** Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

### **UNIT III**

**NETWORK SECURITY PRACTICE:** Authentication Applications, Kerberos, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

### **UNIT IV**

**SYSTEM SECURITY:** Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

### **UNIT V**

**WIRELESS SECURITY:** Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

### **UNIT VI**

**SECURE NETWORKING THREATS:** Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

### **UNIT VII**

**ENCRYPTION TECHNIQUES:** Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

### **UNIT VIII**

**DESIGNING SECURE NETWORKS:** Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security, Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

**TEXT BOOKS:**

1. William Stallings, "Cryptography and Network Security – Principles and Practices", Pearson Education, 3<sup>rd</sup> edition, 2003.
2. Sean Convery, "Network Security Architectures", Published by Cisco Press, 1<sup>st</sup> edition, 2004.

**REFERENCES:**

1. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
2. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", Pearson Education, 3<sup>rd</sup> edition, 2003.
5. Jeff Crume, "Inside Internet Security", Addison Wesley, 2005.

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## **(10MT25707) NANO ELECTRONICS (ELECTIVE II)**

### **UNIT I**

**TECHNOLOGY AND ANALYSIS:** Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

### **UNIT II**

**CARBON NANO STRUCTURES:** Carbon Clusters, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

### **UNIT III**

**LOGIC DEVICES:** Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Field Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

### **UNIT IV**

**RANDOM ACCESS MEMORIES:** High Permittivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

### **UNIT V&VI**

#### **MASS STORAGE DEVICES:**

Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

### **UNIT VII&VIII**

#### **DATA TRANSMISSION, INTERFACES AND DISPLAYS:**

Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

#### **TEXTBOOKS:**

1. Rainer Waser, "Nano Electronics and Information Technology", Wiley VCH, April 2003.
2. Charles Poole, "Introduction to Nano Technology", Wiley Interscience, May 2003.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)**

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## **(10MT25708) REAL TIME OPERATING SYSTEMS (ELECTIVE II)**

### **UNIT I**

**INTRODUCTION TO UNIX:** Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

### **UNIT II&III**

**REAL TIME SYSTEMS:** Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

### **UNIT IV**

**APPROACHES TO REAL TIME SCHEDULING:** Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

### **UNIT V**

**OPERATING SYSTEMS:** Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

### **UNIT VI**

**FAULT TOLERANCE TECHNIQUES:** Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

### **UNIT VII**

**CASE STUDIES-VX WORKS:** Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

### **UNIT VIII**

**RT Linux:** Process Management, Scheduling, Interrupt Management, and Synchronization

### **TEXT BOOKS:**

1. Richard Stevens, "Advanced Unix Programming".
2. Jane W.S. Liu, "Real Time Systems", Pearson Education.
3. C.M.Krishna, KANG G. Shin, "Real Time Systems", McGraw Hill.

### **REFERENCES:**

1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
4. <http://www.xml.com/ldd/chapter/book>

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**(10MT25710) MIXED SIGNAL LABORATORY**

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

**NOTE:** Required Software Tools:

1. Mentor Graphic tools / Cadance tools / Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.

# **SREE VIDYANIKETHAN ENGINEERING COLLEGE**

**(AUTONOMOUS)**

Sree Sainath Nagar, A.Rangampet, Near Tirupati - 517 102. A.P.

## **Salient Features of Prohibition of Ragging in Educational Institutional Act 26 of 1997**

- Ragging within or outside the college is prohibited.
- Ragging means doing an act which causes or is likely to cause insult or annoyance or fear or apprehension or threat or intimidation or outrage of modesty or injury to a student

<b>Nature of Ragging</b>	<b>Punishment</b>
Teasing, Embarrassing and humiliating	Imprisonment up to 6 months or fine up to Rs. 1,000/- or Both
Assaulting or using criminal force or criminal intimidation	Imprisonment up to 1 year or fine up to Rs. 2,000/- or Both
Wrongfully restraining or confining or causing hurt	Imprisonment up to 2 years or fine up to Rs. 5,000/- or Both
Causing grievous hurt, Kidnapping or rape or committing unnatural offence	Imprisonment up to 5 years or fine up to Rs. 10,000/-
Causing death or abetting suicide	Imprisonment up to 10 years or fine up to Rs. 50,000/-

### **Note:**

1. A student convicted of any of the above offences, will be expelled from the College.
2. A student imprisoned for more than six months for any of the above offences will not be admitted in any other College.
3. A student against whom there is prima facie evidence of ragging in any form will be suspended from the College immediately.
4. The full text of Act 26 of 1997 and UGC Regulations on Curbing the Menace of Ragging in Higher Educational Institutions, 2009 **(Dated 17<sup>th</sup> June, 2009)** are placed in the College library for reference.