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Total Marks : 1600
Total Credits: 70
M. Tech. (VLSI)  
I SEMESTER  

(10MT15701) ANALOG IC DESIGN

UNIT I  
MOS transistors-modeling in linear, saturation and cutoff high frequency equivalent circuit.

UNIT II & III  
INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR:  
Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT IV  

UNIT V  
SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

UNIT VI  

UNIT VII  

UNIT VIII  
TEXT BOOKS:

REFERENCES:
UNIT I
HARDWARE MODELING WITH THE VERILOG HDL: Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

UNIT III

UNIT IV
UNIT V

UNIT VI

UNIT VII

UNIT VIII

TEXT BOOKS:

REFERENCES:
UNIT I
CMOS inverters - static and dynamic characteristics.

UNIT II
Static and Dynamic CMOS design - Domino and NORA logic - combinational and sequential circuits.

UNIT III
Method of Logical Effort for transistor sizing - power consumption in CMOS gates - Low power CMOS design.

UNIT IV
Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT V
Bipolar gate Design- BiCMOS logic - static and dynamic behaviour - Delay and power consumption in BiCMOS Logic.

UNIT VI&VII
LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load.

UNIT VIII
SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth’s algorithm.

TEXT BOOKS:

REFERENCES:
UNIT I
CO-DESIGN ISSUES: Co-Design Models, Architectures, Languages, a Generic Co-design Methodology.

UNIT II
CO-SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware-software partitioning distributed system co-synthesis.

UNIT III
PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT IV
TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT V
COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI
DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT VII
LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-I: System - level specification, design representation for system level synthesis, system level specification languages,

UNIT VIII
LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:
SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)

M. Tech. (VLSI)
I SEMESTER

(10MT15705) VLSI TECHNOLOGY

UNIT I
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

UNIT II
BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds Relationships, Threshold Voltage \( V_t \), \( G_m \), \( G_{ds} \) and \( W_0 \), Pass Transistor, MOS,CMOS & Bi- CMOS Inverters, \( Z_{pu}/Z_{pd} \), MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT III

UNIT IV

UNIT V

UNIT VI
SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VII

UNIT VIII
INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware-Software Co-design, Chip Design Methodologies- A simple Design Example.

TEXT BOOKS:
REFERENCES:
UNIT I
ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

UNIT II

UNIT III
ASICs – DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

UNIT IV
ACISS CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs,Mixed mode and analogue ASICs.

UNIT V
ASIC DESIGN TECHNIQUES: Overview- Design flow and methodology- Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA

UNIT VI
LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation.

UNIT VII
ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

UNIT VIII
FPGA PARTITIONING: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

REFERENCES:
UNIT I
AN INTRODUCTION TO EMBEDDED SYSTEMS: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System-On-Chip (SOC) and in VLSI Circuit.

UNIT II:
PROCESSOR AND MEMORY ORGANIZATION: Structural Units In a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded Systems, Allocation of Memory to Program Cache and Memory Management Links, Segments and Blocks and Memory Map of a System, DMA, Interfacing Processors, Memories and Input Output Devices.

UNIT III

UNIT IV
DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM: Device Drivers, Parallel Port and Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing Mechanism.

UNIT V
INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VI
PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++ AND JAVA: Interprocess Communication and Synchronization of Processes, Task and Threads, Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Interprocess Communication.

UNIT VII & VIII
TEXTBOOKS:
1. Rajkamal, “Embedded systems: Architecture, Programming and Design”, TMH.
2. Wayne wolf, “Computers as a component: principles of embedded computing system design”.

REFERENCES:
1. Arnold S Burger, “Embedded system design”, CMP.
2. David Simon, “An embedded software primer”, PEA.
4. Hayt, “Data communication”.

UNIT I

UNIT II
SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT III
BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

UNIT IV
MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT V
EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

UNIT VI

UNIT VII
EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT VIII
SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

REFERENCES:
 DIGITAL IC DESIGN LABORATORY

- Digital Circuits Description using Verilog and VHDL.
- Verification of the Functionality of Designed circuits using function Simulator.
- Timing Simulation for critical path time calculation.
- Synthesis of Digital circuits.
- Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
- Implementation of Designed Digital Circuits using FPGA and CPLD devices.

**NOTE:** Required Software Tools:
- Mentor Graphic tools / Cadence tools/ Synopsis tools. (220 nm Technology and Above)
- Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.
UNIT I
PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III
Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV
MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V
LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

UNIT VI

UNIT VII
PHYSICAL DESIGN AUTOMATION OF FPGA’S: FPGA technologies, Physical Design cycle for FPGA’s, partitioning and Routing for segmented and staggered Models.

UNIT VIII
PHYSICAL DESIGN AUTOMATION OF MCM’S: MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM’s.

TEXTBOOKS:
REFERENCES:
UNIT I

UNIT II

UNIT III
CASE STUDIES: Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT & T-ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s – ACT-1,2,3 and Their Speed Performance.

UNIT IV
FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT V

UNIT VI & VII

UNIT VIII
TEXT BOOKS/ REFERENCES:
UNIT I

UNIT II

UNIT III

UNIT IV&V

UNIT VI

UNIT VII
MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

UNIT VIII

TEXT BOOKS:
REFERENCES:
SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)

M. Tech. (VLSI)  L  T  P  C  II SEMESTER  4  -  -  4

(10MT25704) LOW POWER VLSI DESIGN

UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low-voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

UNIT III
LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V
CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII
SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

REFERENCES:
UNIT I
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II & III
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT IV & V
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT VI & VII
Debugger Internal &Externals Portable Functions. Extensive Exercises for Programming in PERL.

UNIT VIII
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

TEXT BOOKS:
SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)

M. Tech. (VLSI) II SEMESTER

(10MT25706) CRYPTOGRAPHY AND NETWORK SECURITY (ELECTIVE II)

UNIT I

UNIT II

UNIT III

UNIT IV

UNIT V

UNIT VI

UNIT VII
ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT VIII
TEXT BOOKS:

REFERENCES:
UNIT I
TECHNOLOGY AND ANALYSIS: Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

UNIT II

UNIT III

UNIT IV
RANDOM ACESS MEMORIES: High Permittivity Materials for DRAMs, Ferro Electric Random Access Memories, Magneto-Resistive RAM.

UNIT V&VI
MASS STORAGE DEVICES:
Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT VII&VIII
DATA TRANSMISSION, INTERFACES AND DISPLAYS:
Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:
(10MT25708) REAL TIME OPERATING SYSTEMS (ELECTIVE II)

UNIT I
INTRODUCTION TO UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT II & III

UNIT IV
APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT V

UNIT VI

UNIT VII
CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT VIII
RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

REFERENCES:
1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
1. Analog Circuits Simulation using Spice.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
7. Design Rule Checks.

**NOTE:** Required Software Tools:

1. Mentor Graphic tools / Cadance tools / Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.
Salient Features of Prohibition of Ragging in Educational Institutional Act 26 of 1997

- Ragging within or outside the college is prohibited.
- Ragging means doing an act which causes or is likely to cause insult or annoyance or fear or apprehension or threat or intimidation or outrage of modesty or injury to a student.

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<td>Teasing, Embarrassing and humiliating</td>
<td>Imprisonment up to 6 months or fine up to Rs. 1,000/- or Both</td>
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<tr>
<td>Assaulting or using criminal force or criminal intimidation</td>
<td>Imprisonment up to 1 year or fine up to Rs. 2,000/- or Both</td>
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<td>Wrongfully restraining or confining or causing hurt</td>
<td>Imprisonment up to 2 years or fine up to Rs. 5,000/- or Both</td>
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<td>Causing grievous hurt, Kidnapping or rape or committing unnatural offence</td>
<td>Imprisonment up to 5 years or fine up to Rs. 10,000/-</td>
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<td>Causing death or abetting suicide</td>
<td>Imprisonment up to 10 years or fine up to Rs. 50,000/-</td>
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**Note:**

1. A student convicted of any of the above offences, will be expelled from the College.
2. A student imprisoned for more than six months for any of the above offences will not be admitted in any other College.
3. A student against whom there is prima facie evidence of ragging in any form will be suspended from the College immediately.
4. The full text of Act 26 of 1997 and UGC Regulations on Curbing the Menace of Ragging in Higher Educational Institutions, 2009 (Dated 17th June, 2009) are placed in the College library for reference.