# Course Structure for M. Tech. (DECS)

## M. Tech. – I Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Name of the Subject</th>
<th>L+T</th>
<th>P</th>
<th>Internal Marks</th>
<th>External Marks</th>
<th>Total Marks</th>
<th>C</th>
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<tbody>
<tr>
<td>10MT13801</td>
<td>Advanced Digital Signal Processing</td>
<td>4</td>
<td></td>
<td>40</td>
<td>60</td>
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<tr>
<td>10MT13802</td>
<td>Digital Communication Techniques</td>
<td>4</td>
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<tr>
<td>10MT13803</td>
<td>Digital System Design</td>
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<td>10MT13804</td>
<td>Embedded Systems</td>
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<td>10MT13805</td>
<td>Microcomputer System Design</td>
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**Elective-I**

<table>
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<tr>
<th>Subject Code</th>
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<th>Internal Marks</th>
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<tr>
<td>10MT13806</td>
<td>Advanced Computer Architectures</td>
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<tr>
<td>10MT13807</td>
<td>DSP Processors and Architectures</td>
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<td>10MT13808</td>
<td>Low Power VLSI Design</td>
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<td>Digital Systems Design Lab.</td>
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**Total** 24 4 265 410 675 26

## M. Tech. – II Semester

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<tr>
<td>10MT23801</td>
<td>Adaptive Signal Processing</td>
<td>4</td>
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<tr>
<td>10MT23802</td>
<td>Coding Theory and Techniques</td>
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<td>Detection and Estimation of Signals</td>
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<td>Wireless Communications</td>
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**Elective-II**

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<tr>
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<tr>
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**Total** 24 4 315 410 725 28

## M. Tech. – III Semester

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<th>Name of the Subject</th>
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<td>Project Work – Phase I</td>
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**Total** 50 - 50 4

## M. Tech. – IV Semester

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<td>Project Work – Phase II</td>
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**Total** 50 100 150 12

Total Marks : 1600
Total Credits: 70
UNIT I

UNIT II
LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple Digital Filters, Complementary Transfer Function, Inverse Systems, System Identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT III

UNIT IV

UNIT V
MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT VI
POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

UNIT VII
PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.
UNIT VIII

TEXTBOOKS:

REFERENCES:
UNIT I

UNIT II

UNIT III
DIGITAL MODULATION TECHNIQUES: Factors that Influence digital modulation techniques, Linear Modulation Techniques – BPSK, DPSK, QPSK, OQPSK, ∏/4 QPSK, Constant envelope Modulation techniques - MSK, GMSK, Linear and constant envelope modulation techniques – M-ary PSK, M-ary QAM.

UNIT IV
COMMUNICATION OVER ADDITIVE GAUSSIAN NOISE CHANNELS: Optimum receiver for signals corrupted by AWGN, Performance of the optimum Receiver for Memory less Modulation, Optimum Receiver for CPM signals, Optimum Receiver for Signals with Random Phase in AWGN Channel.

UNIT V
CARRIER RECOVERY AND SYMBOL SYNCHRONIZATION: Carrier recovery and symbol synchronization in Signal demodulation, Phase locked loop, Effect of additive noise in phase estimation, non-decision directed loops, symbol timing estimation.

UNIT VI
COMMUNICATION THROUGH BAND LIMITED LINEAR FILTER CHANNELS: Optimum Receiver for Channels with ISI and AWGN, Linear Equalization and its Variations, Decision Feedback Equalization.

UNIT VII

UNIT VIII
SYNCHRONIZATION OF SPREAD SPECTRUM SYSTEMS: Coherent Direct-Sequence Receivers, Carrier Tracking- Coherent & Non Coherent, Delay-Lock Loop Analysis, Tau-Dither Loop, Acquisition of Spread-Spectrum Signals, Matched filters for PN Sequences.
Text Books:

References:
UNIT I
DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT II
SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT III
FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.
TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT IV
TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature Analysis and testing for bridging faults.

UNIT V

UNIT VI
PROGRAMMING LOGIC ARRAYS: Design using PLA’s, PLA minimization and PLA folding.

UNIT VII
PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT VIII
ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:
1. Z. Kohavi, “Switching & finite Automata Theory”, TMH.
2. N. N. Biswas, “Logic Design Theory”, PHI.

REFERENCES:
2. Charles H. Roth Jr., “Fundamentals of Logic Design”.
UNIT I
**INTRODUCTION:** Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

UNIT II

UNIT III
**SURVEY OF SOFTWARE ARCHITECTURE:** Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

UNIT IV
**EMBEDDED SOFTWARE DEVELOPMENT TOOLS:** Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique.

UNIT V
**RTOS CONCEPTS:** Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT VI
**INSTRUCTION SETS:** Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII
**SYSTEM DESIGN TECHNIQUES:** Design methodologies, requirement analysis, specifications, system analysis and architecture design.

UNIT VIII
**DESIGN EXAMPLES:** Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

**TEXT BOOKS:**
1. Wayne Wolf, “Computers as a component: principles of embedded computing system design”.

**REFERENCES:**
UNIT I
REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.

UNIT II
THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT III
THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT IV

UNIT V
THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

UNIT VI
I/O PROGRAMMING: Fundamentals of I/O Considerations Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

UNIT VII
INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT VIII
ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

TEXTBOOKS:
2. A.K.Ray and K.M.Bhurchandi, “Advanced Microprocessor and Peripherals”, TMH.

REFERENCES:
UNIT I
**FUNDAMENTALS OF COMPUTER DESIGN:** Technology trends, cost-measuring and reporting performance quantitative principles of computer design.

UNIT II
**INSTRUCTION SET PRINCIPLES AND EXAMPLES:** classifying instruction set- memory addressing- type and size of operands-addressing modes for signal processing-operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler

UNIT III
**INSTRUCTION LEVEL PARALLELISM (ILP):** over coming data hazards- reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

UNIT IV
**ILP SOFTWARE APPROACH:** compiler techniques- static branch protection, VLIW approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V
**MEMORY HIERARCHY DESIGN:** cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI
**MULTIPROCESSORS AND THREAD LEVEL PARALLELISM:** symmetric shared memory architectures, distributed shared memory, Synchronization, multithreading.

UNIT VII
**STORAGE SYSTEMS:** Types, Buses, RAID, errors and failures, benchmarking a storage device, designing a I/O system.

UNIT VIII
**INTER CONNECTION NETWORKS AND CLUSTERS:** interconnection network media, practical issues in interconnecting networks- examples, clusters, designing a cluster

**TEXT BOOKS:**

**REFERENCES:**
UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV
EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI
IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII
IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.
UNIT VIII
INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

REFERENCES:
SREE VIDYANIKETHAN ENGINEERING COLLEGE (AUTONOMOUS)

M. Tech. (DECS) L T P C
I SEMESTER 4 - - 4

(10MT13808) LOW POWER VLSI DESIGN
(ELECTIVE I)

UNIT I
LOW POWER DESIGN, AN OVER VIEW: Introduction to low-voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

UNIT III
LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV
DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V
CMOS AND BI-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI
LOW-VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII
SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

REFERENCES:
CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.
3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.
5. Design and Simulation of Counters- Ring Counter, Johnson Counter, and Up- Down Counter, Ripple Counter.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
8. 4- Bit Multiplier, Divider. (for 4-Bit Operand)
9. Design ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s COMPLIMENT, Multiplication, Division.

CYCLE 2: After Digital Circuit Description Using Verilog/ VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
4. Place and Router Techniques for FPGA’s like Xilinx, Altera, Cypress, etc.,
UNIT I
EIGEN ANALYSIS: Eigen Value Problem, Properties of eigen values and eigen vectors, Eigen Filters, eigen Value computations.

UNIT II
INTRODUCTION TO ADAPTIVE SYSTEMS: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner - Description, Weight Vectors, Desired Response Performance function, Gradient & Mean Square Error.

UNIT III

SEARCHING THE PERFORMANCE SURFACE – Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability & Rate of convergence - Learning Curves.

UNIT IV
STEEPEST DESCENT ALGORITHMS: Gradient Search by Newton’s Method, Method of Steepest Descent, Comparison of Learning Curves.

UNIT V

UNIT VI
RLS ALGORITHM: Matrix Inversion lemma, Exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, convergence analysis of RLS Algorithm, Application of RLS algorithm on Adaptive Equalization

UNIT VII
UNIT VIII
NON LINEAR ADAPTIVE FILTERING: Theoretical and Practical considerations of Blind Deconvolution, Buss Gang Algorithm for blind Equalization of real base band Channels.

TEXT BOOKS:

REFERENCES:
UNIT I
SOURCE CODING: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for Discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes.

UNIT II
Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

UNIT III
LINEAR BLOCK CODES: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes.

UNIT IV
Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

UNIT V
CYCLIC CODES: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

UNIT VI
CONVOLUTIONAL CODES: encoding of Convolutional codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.

UNIT VII
Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

UNIT VIII
BCH CODES: Groups, fields, binary Fields arithmetic, construction of Galois fields GF (2^m), Basic properties of Galois Fields, Computation using Galois Field GF (2^m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.
TEXT BOOKS:

REFERENCES:
UNIT I
DETECTION THEORY: Binary decisions - Single observation- Maximum likelihood decision criterion, Neymann-Pearson criterion, Probability of error criterion, Bayes risk criterion, Minimax criterion, Robust detection, Receiver operating characteristics.

UNIT II&III
BINARY DECISIONS - MULTIPLE OBSERVATIONS: Vector observations, the general Gaussian Problem, Waveform Observation in Additive Gaussian Noise, The Integrating Optimum Receiver; Matched Filter Receiver.

UNIT IV&V
ESTIMATION THEORY: Methods -Maximum likelihood estimation; Bayes cost method Bayes estimation criterion - Mean square error criterion; Uniform cost function; absolute value cost function; Linear minimum variance - Least squares method; Estimation in the presence of Gaussian noise - Linear observation; Non-linear estimation.

UNIT VI
PROPERTIES OF ESTIMATORS: Bias, Efficiency, Cramer Rao bound Asymptotic properties, Sensitivity and error analysis.

UNIT VII
STATE ESTIMATION: Prediction, Kalman filter.

UNIT VIII
SUFFICIENT STATISTICS AND STATISTICAL ESTIMATION OF PARAMETERS: Concept of sufficient statistics, Exponential families of Distributions, Exponential families and Maximum likelihood estimation, uniformly minimum variance unbiased estimation.

TEXT BOOKS:

REFERENCES:
UNIT I
NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture.

UNIT II
ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III
ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections.

UNIT IV
QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT V

UNIT VI
REARRANGEABLE NETWORKS: Rearrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT VII
ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.

UNIT VIII
TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active, QOS in IP networks: differentiated and integrated services.

TEXT BOOKS:
UNIT I
INTRODUCTION TO WIRELESS COMMUNICATIONS SYSTEMS: Evolution, Examples of wireless communications systems, Comparison, Second Generation Cellular Networks, WLL, Bluetooth and Personal Area networks.

UNIT II
LARGE SCALE PATH LOSS AND SHADOWING: Introduction to radio wave propagation, Free Space Propagation Model, Propagation mechanisms, Reflection, Ground Reflection (Two Ray) model, Diffraction, Scattering, outdoor Propagation Model and Indoor Propagation model.

UNIT III

UNIT IV

UNIT V
CELLULAR CONCEPT- SYSTEM DESIGN FUNDAMENTALS: Frequency reuse, Channel assignment strategies, Handoff strategies, Interface and System Capacity—Co-channel Interface and System Capacity, Capacity of Cellular CDMA, Capacity of CDMA with Multiple Cells, Channel Planning for Wireless systems, Adjacent channel interface, Trunking and Grade of Service, Improving Capacity-Cell Splitting and Sectorization,

UNIT VI
ACCESS AND DUPLEX TECHNIQUES: FDMA, TDMA, Frame Slot Format for TDMA Systems, Super Frame Format, Synchronization of Slot, Frame & Super Frame, CDMA, Near Far Problem and Power Control, Synchronization Specific for CDMA, Comparison of FDMA, TDMA and CDMA, FDD&TDD.

UNIT VII
INTRODUCTION TO SPACE-TIME WIRELESS COMMUNICATIONS: Introduction, Exploiting Multiple antennas in wireless links, Space-Time (ST) Channel and Signal Models-SIMO, MISO, MIMO Channels, Physical Scattering Models for ST Channels, Sampled Signal Model, Capacity of ST Channels-Capacity of Frequency flat deterministic MIMO channel, Channel unknown & known to the transmitter, Capacity of random MIMO channels, Capacity to frequency selective MIMO channels.
UNIT VIII

TEXT BOOKS:

REFERENCES:
UNIT I & II
REVIEW OF INFORMATION THEORY: The discrete memoryless information source, Kraft inequality; optimal codes Source coding theorem. Compression Techniques, Lossless and Lossy Compression, Mathematical Preliminaries for Lossless Compression, Huffman Coding, Optimality of Huffman codes, Extended Huffman Coding, Adaptive Huffman Coding, Arithmetic Coding, Adaptive Arithmetic coding, Run Length Coding.

UNIT III

UNIT IV
MATHEMATICAL PRELIMINARIES FOR LOSSY CODING: Rate distortion theory: Rate distortion function R(D), Properties of R(D); Calculation of R(D) for the binary source and the Gaussian source, Rate distortion theorem, Converse of the Rate distortion theorem.

UNIT V
QUANTIZATION: Uniform & Non-uniform, optimal and adaptive quantization, vector quantization and structures for VQ, Optimality conditions for VQ, Predictive Coding, Differential Encoding Schemes.

UNIT VI

UNIT VII

UNIT VIII
IMAGE COMPRESSION STANDARDS: Binary Image Compression Standards, Continuous Tone Still Image Compression Standards, Video Compression Standards.

TEXT BOOKS:
REFERENCES:
UNIT I
**IMAGE REPRESENTATION:** Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II
**IMAGE ENHANCEMENT:** Filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge detection, non parametric and model based approaches, LOG filters, localization problem.

UNIT III
**IMAGE RESTORATION:** Degradation Models, PSF, circulant and block-circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT IV
**IMAGE SEGMENTATION:** Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Edge detection, Hough transform, Region growing.

UNIT V
**FUNDAMENTAL CONCEPTS OF IMAGE COMPRESSION:** Compression models, Information theoretic perspective, Fundamental coding theorem.

UNIT VI
**LOSSLESS COMPRESSION:** Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT VII
**VIDEO PROCESSING:** Representation of Digital Video, Spatio-temporal sampling, Motion Estimation.

UNIT VIII
Video Filtering, Video Compression, Video coding standards.

**TEXT BOOKS/REFERENCES:**
UNIT I
INTRODUCTION: Evolution of fiber types, guiding properties of fibers, cross talk between fibers, coupled modes and mode mixing, dispersion properties of fibers, nonlinear properties of optical fibers, SRS, SBS, intensity dependent refractive index.

UNIT II
OPTICAL AND MECHANICAL CHARACTERIZATION OF FIBERS
Fiber design considerations: diameter, cladding, thickness, low and high bit rate systems, characterization of materials for fibers, fiber perform preparation, fiber drawing and control, roles of coating and jacketing.

UNIT III
OPTICAL CABLE DESIGN: Design objectives and cable structures, fiber splicing, fiber end preparation, single and array splices, measurement of splicing efficiency, optical fiber connectors, Connector alignments.

UNIT IV
OPTICAL SOURCES AND DETECTORS: optical sources for communication, LED, injection lasers, modulation technique, direct and indirect methods, optical waveguide devices. Photodiodes in repeaters, receiver design, digital and analog, transmission system design, system design choices, passive and low speed active optical components for fiber system, micro-optic components, lens-less components.

UNIT V
OPTICAL FIBER COMPONENTS: couplers, Isolators and Circulators, Multiplexers, Bragg grating, Fabry-perot Filters, Mach zender interferometers, Arrayed waveguide grating, tunable filters, hi-channel count multiplexer architectures, optical amplifiers, direct and external modulation transmitters, pump sources for amplifiers, optical switching and wave length converters.

UNIT VI
OPTICAL FIBER TECHNIQUES: Modulation and demodulation, signal formats, direction detection receivers, coherent detection.

UNIT-VII
ACCESS NETWORK: Network architecture, HFC, FTTC, optical access network architecture, deployment considerations, upgrading the transmission capacity, SDM, TDM, WDM, application areas, inter exchange, undersea, local exchange networks; Packaging and cabling of photonics components- photonic packet switching, OTDM, multiplexing and demultiplexing, optical logic gates, synchronization, broadcast OTDM network, OTDM testbeds.
UNIT-VIII
SOLITON COMMUNICATION: Basic principle, metropolitan optical network, cable TV network, optical access network, photonics simulation tools, error control coding techniques, nonlinear optical effects in WDM transmission.

TEXT BOOKS:

REFERENCES:
2. Govind Agarwal, “Optical Fiber Communications”.
1. Simulation Rayleigh Fading Channel Using Either Clarke’s Model or Jake’s Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
3. Design and Simulation FIR Filter Using any Windowing Technique.
4. Design of IIR Filters from Analog Filters.
5. Performance Evaluation of QPSK System over Gaussian AWGN Channel.
7. Equalization of Multipath Channel using LMS or RLS Algorithms.
8. Performance Evaluation of RAKE Receiver over Slow Fading Channel.

**NOTE:** Use Matlab / COM SIM.
Salient Features of Prohibition of Ragging in Educational Institutional Act 26 of 1997

- Ragging within or outside the college is prohibited.
- Ragging means doing an act which causes or is likely to cause insult or annoyance or fear or apprehension or threat or intimidation or outrage of modesty or injury to a student.

<table>
<thead>
<tr>
<th>Nature of Ragging</th>
<th>Punishment</th>
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<tbody>
<tr>
<td>Teasing, Embarrassing and humiliating</td>
<td>Imprisonment up to 6 months or fine up to Rs. 1,000/- or Both</td>
</tr>
<tr>
<td>Assaulting or using criminal force or criminal intimidation</td>
<td>Imprisonment up to 1 year or fine up to Rs. 2,000/- or Both</td>
</tr>
<tr>
<td>Wrongfully restraining or confining or causing hurt</td>
<td>Imprisonment up to 2 years or fine up to Rs. 5,000/- or Both</td>
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<tr>
<td>Causing grievous hurt, Kidnapping or rape or committing unnatural offence</td>
<td>Imprisonment up to 5 years or fine up to Rs. 10,000/-</td>
</tr>
<tr>
<td>Causing death or abetting suicide</td>
<td>Imprisonment up to 10 years or fine up to Rs. 50,000/-</td>
</tr>
</tbody>
</table>

Note:

1. A student convicted of any of the above offences, will be expelled from the College.
2. A student imprisoned for more than six months for any of the above offences will not be admitted in any other College.
3. A student against whom there is prima facie evidence of ragging in any form will be suspended from the College immediately.
4. The full text of Act 26 of 1997 and UGC Regulations on Curbing the Menace of Ragging in Higher Educational Institutions, 2009 (Dated 17th June, 2009) are placed in the College library for reference.