

# SREE VIDYANIKETHAN ENGINEERING COLLEGE

Sree Sainath Nagar, A.Rangampet – 517 102

## TIME TABLE

2010 – 2011

### ELECTRICAL & ELECTRONICS ENGINEERING III – B.TECH., SECTION-A (I- SEMESTER)

Room No: 115

With effect from:01-07-2010

Hour	8:00-8:50	8:50-9:40	9:40-10:30		11:00-11:50	11:50-12:40	12:40-1:30
Day	1	2	3	B	4	5	6
MON	PS-II	EM-III	LSA	R	PE	CSO	EM
TUE	CSO	EM	PS-II		LSA	PE	EM-III
WED	EM-II/CS Lab			E	EM-III	PS-II	CSO
THU	LSA	CSO	EM-III	A	PS-II	EM	PE
FRI	EM	PE	LSA		CS/EM-II Lab		
SAT	EM-III	LSA	CSO	K	EM	PE	PS-II

CSO	:	Computer Systems Organization	Dr. K. Ramani
PS – II	:	Power system – II	Mr. T. Kosaleswara Reddy
EM – III	:	Electrical Machines –III	Mr. A. Munisankar
EM	:	Electrical Measurements	Mr. N. Sreekanth
PE	:	Power Electronics	Mr. P. Ramesh
LSA	:	Linear System Analysis	Mr. M. Saravanan
EM – II LAB	:	Electrical Machines – II Lab	Mr. P. Ramesh Mr. T. Kosaleswara Reddy /Mr. A. Munisankar
CS&S LAB	:	Control Systems & Simulation Lab	Mr. N. Sreekanth Ms. T. Susritha

Date: 01-07-10

HEAD

PRINCIPAL

Batch 1: 08121A0201 – 237

Batch 2: 08121A0238 - 275

#### Copy to:

1. The Principal's Office
2. The Examination Cell
3. HOD EEE