

SREE VIDYANIKETHAN ENGINEERING COLLEGE
Sree Sainath Nagar, Tirupati- 517 102

YEAR 2009 – 2010

TIME – TABLE

Department of Electronics & Communication Engineering

M.Tech. I-Semester (VLSI)

Room No. **716**

w.e.f: **19-10-2009**

DAY / Hour	09:00 to 12:20			L U N C H	01:25 -	02:15 -	03:05 -	03:55 -
	4 Periods				02:15	03:05	03:55	04:45
					4	5	6	7
MON	Digital IC Design Lab				HDL	DID	HSD	AIC
TUE	/				ASIC	AIC	VLSI	DID
WED					ASIC	HSD	HDL	DID
THU					ASIC	HDL	VLSI	HSD
FRI					ASIC	DID	VLSI	AIC
SAT					HSD	HDL	AIC	VLSI

VLSI	VLSI Technology	Mr. D.Damodaram
AID	Analog Ic Design	Ms.C.M.Sripriya
DID	Digital Ic Design	Ms. P.Anitha
HDL	Hardware Description Languages	Mr. P.Madhu Kumar
HSD	Hardware Software co-design	Mr. S.V.S.Jaya Shayam
ASIC	ASIC Design	Dr. Sk.Noor Mahammad
DID LAB	Digital IC Design Lab	Dr.Sk.Noor Mahammad & Ms.C.M.Sripriya

Head, Dept. of ECE

Principal

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 Examination Section
 Director PG.Courses.