

SREE VIDYANIKETHAN ENGINEERING COLLEGE
Sree Sainath Nagar, Tirupati- 517 102

YEAR 2009 – 2010

TIME – TABLE

Department of Electronics & Communication Engineering

M.Tech. I-Semester (Digital Electronics & Communication Systems)

Room No. **616**

w.e.f: **19-10-2009**

DAY / Hour	09:00 to 12:20			L U N C H	01:25 -	02:15 -	03:05 -	03:55 -
	4 Periods				02:15	03:05	03:55	04:45
					5	6	7	8
MON	Digital System Design Lab				ACA	ESC	DSD	ASP
TUE					DCT	ACA	ASP	DSD
WED					DCT	ADSP	ASP	ESC
THU					ADSP	ACA	DCT	DSD
FRI					ASP	ESC	ADSP	DCT
SAT					ACA	ESC	DSD	ADSP

DSD	Digital System Design	Mr. R. Nagendra
ADSP	Advanced Digital Signal Processing	Ms. D. Leela Rani
ESC	Embedded System Concepts	Mr. T. Syama Sundara
DCT	Digital Communication Techniques	Ms. V.R. Anitha
ASP	Adaptive Signal Processing	Mr.T.V.S. Gowtham Prasad
ACA	Advanced Computer Architectures	Dr.Sk.Noor Mahammad
DSD LAB	Digital System Design Lab	Mr.R.Nagendra & Mr.S.V.S.Jaya Shyam

Head, Dept. of ECE

Principal

Copy to : Principal's Office
Examination Section
Director PG.Courses.