

SREE VIDYANIKETHAN ENGINEERING COLLEGE

SREE SAINATH NAGAR, A. RANGAMPET – 517 102

Department Of Computer Science and Systems Engineering

TIME TABLE

(2010-2011)

II B. TECH I Semester

ROOM NO: **711**

w.e.f. **01.07.2010**

DAY/ HR	10:30-11:20 1	11:20-12:10 2	12:10-1:00 3		2:15-3:05 4	3:05-3:55 5	3:55-4:45 6
MON	BEE	EDC	ES	L U N C H B R E A K	MFCS	DLD&CO	ADSA
TUE	EDC	BEE	DLD&CO		ES	ADSA	MFCS
WED	MFCS	ADSA	EDC		EE LAB (TKR, SR)		
THU	ADSA LAB (C& D) (AC, PDL, KL, PLN, KH)				ES	BEE	DLD&CO
FRI	ES	ADSA	DLD&CO		BEE	MFCS	EDC
SAT	ADSA	MFCS	ES		EDC	DLD&CO	BEE

DLD & CO	DIGITAL LOGIC DESIGN & COMPUTER ORGANIZATION	MR. K. HAJARATAIAH
ADSA	ADVANCED DATA STRUCTURES AND ALGORITHMS	MR. A. CHANDRA
MFCS	MATHEMATICAL FOUNDATIONS OF COMPUTER SCIENCE	MR. P. LAKSHMI NARAYANA
ES	ENVIRONMENTAL STUDIES	MS. D.SUMALATHA
BEE	BASIC ELECTRICAL ENGINEERING	MR.T.KOSALESWARA REDDY
EDC	ELECTRONIC DEVICES AND CIRCUITS	RAVINDRA MURTY
ADSA LAB	ADVANCED DATA STRUCTURES AND ALGORITHMS LAB	AC, PDL, KL, PLN, KH
EE LAB	ELECTRICAL AND ELECTRONICS LAB	TKR, SR

HOD

PRINCIPAL